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EXAMINER	
PEUGH, BRIAN R	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 06/03/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/539,839	BERKOVITS, ARIEL	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Prosecution Application

The request filed on April 9, 2003 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/539,839 is acceptable and a CPA has been established. An action on the CPA follows.

Claim Objections

Claims 1-8, 17-24, and 30 are objected to because of the following informalities:

Claim 1, line 2 recites an "instruction *to access* valid data in a cache" (emphasis added). The third line of claim 1 then recites that the instruction is to "indicate that a line storing *the accessed* valid data in the cache" (emphasis added). While the second line only recites an instruction for accessing valid data, the third line seems to indicate to the Examiner that the valid data of the second line has actually been accessed. The Applicant is encouraged to amend the claim language in order to link the "instruction to access valid data" with the "accessed valid data" line, if that is the intent of the claimed subject matter.

Claim 17 recites the same subject matter previously referenced in lines 3-4.

Claim 30 recites the same subject matter previously referenced in lines 2-3.

Claims 2-8 and 18-24 are objected to as being dependent upon an objected claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 9, 10, 25-27, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Genduso et al. (US# 5,778,422).

Genduso et al. teaches a caching system with a memory controller for processing read and write cache operations. Write-Allocate/Read-Invalidate (WA/RI) cache (48) responds to a read request by determining whether the requested data is found within the cache. If the data is found, the read invalidate operation/instruction occurs. Genduso et al. teaches that once the full requested cache line is sent to the CPU, memory controller (20) writes-back the requested WA/RI cache line to main memory and invalidates the requested cache line in the WA/RI cache (col. 8, line 67 – col. 9, line 17; Figs. 2 & 6). Thus, a cache line is invalidated (which necessitates that a valid cache line was accessed) and becomes available for replacement as having a reduced importance level when compared to that of a valid cache line.

Specifically regarding claim 25, memory controller (20) corresponds to the claimed subject matter of the cache control logic, in that the memory controller is responsible for the writing-back of data to the main memory and invalidation of the cache line based upon the read invalidation operation/instruction.

Specifically regarding claim 26, the invalidation of the cache line due to the read invalidate operation/instruction is an indicator that the cache line no longer contains useful data and can be replaced.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Genduso et al. (US# 5,778,422).

Genduso et al. teaches a caching system with a memory controller for processing read and write cache operations. Write-Allocate/Read-Invalidate (WA/RI) cache (48) responds to a read request by determining whether the requested data is found within the cache. If the data is found, the read invalidate operation occurs. Genduso et al. teaches that once the full requested cache line is sent to the CPU, memory controller (20) writes-back the requested WA/RI cache line to main memory and invalidates the requested cache line in the WA/RI cache (col. 8, line 67 – col. 9, line 17; Figs. 2 & 6). Thus, a cache line is invalidated (which necessitates that a valid cache line was accessed) and becomes available for replacement as having a reduced importance level when compared to that of a valid cache line.

Genduso et al., however, does not specifically recite a machine-readable medium having stored thereon a plurality of executable instructions to perform the invalidation and importance level reduction as claimed. However, one of ordinary skill in the art would have recognized that machine-readable medium (disk drive, ROM, RAM, etc.) carry machine-, or computer-, readable instructions for implementing a method, because then it would facilitate the transporting and installing of the method on other systems, as is generally well-known in the art. For example, a copy of the Microsoft Windows Operating System can be found on a cd-rom, from which the Operating System can be installed onto other systems, which is easier than incorporating a long cable or hand typing the software onto another system. The Examiner takes Official Notice of this teaching. Therefore, it would have been obvious to put Genduso et al.'s instructions on a machine-readable medium, because it would facilitate the transporting installing and implementing of Genduso et al.'s instructions on another system.

Claims 3-5, 11-13, 19-21, 28, and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by over Genduso et al. (US# 5,778,422) and Csoppenszky (US# 5,802,568).

Regarding claims 5, 13, and 29, Genduso et al. teaches that according to the read-invalidation instruction, the most-recently-used (MRU) cache item is marked invalid for replacement.

The difference between the claimed subject matter is that claims recite that the reducing of the importance level results in the cache line being replaced prior to other

lines scheduled for replacement (claims 3, 11, 19, and 28) in an LRU-based replacement system (claims 4, 12, and 20) which in effect alters the allocation methodology of the cache (claims 5, 13, 21, and 29).

Regarding claims 3, 11, 19, and 28, Csoppenszky teaches an LRU process incorporating a validity indicator for each cache line. If a cache is full when a write operation is required to place data into the cache, an invalid entry or the LRU entry is picked for replacement (col. 1, lines 43-46). Also, the invalid entries are overwritten first in the simplified LRU process as taught by Csoppenszky (col. 1, lines 58-61). If all of the entries are found to be valid, one of the cache entries which does not have its associated used by set is selected to be overwritten. Thus, non-used entries are replaced prior to invalidated entries, which are replaced prior to valid entries according to the simplified LRU scheme.

Regarding claims 4, 12, and 20, Csoppenszky teaches that the process for determining cache replacement entries is based upon a simplified LRU process, as recited in the previous paragraph. As recited above, the clearing of the used bit makes it possible that the least recently used item may not be selected before another item that was more recently used.

Regarding claims 5, 13, 21, and 29, since all lines of Csoppenszky, having had their used bits cleared, the used and validity bits do not indicate the order in which entries where used or which entry was least recently used, an item selected for replacement (with used bit cleared) could have been selected before another item (with

used bit cleared) according to the LRU policy (col. 1, line 61 – col. 2, line 1). Thus, the allocation methodology according to the LRU policy has been altered.

Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Genduso et al. and Csoppenszky before him at the time the invention was made to modify the caching system of Genduso et al. to include the simplified LRU system of Csoppenszky, because then a cache-replacement policy could be implemented to restrict the cache from removing what is thought to be the most frequently used data unless under specific circumstances, as taught by Csoppenszky.

Claims 6, 7, 14, 15, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Genduso et al. (US# 5,778,422), Csoppenszky (US# 5,802,568), and Funk et al. (US# 6,314,561).

The difference between the claimed subject matter and that of Genduso et al. and Csoppenszky, disclosed supra, is that the claims recite that the replacement instruction is generated by a compiler (claims 7, 15, and 23) or is part of an application kernel (claims 6, 14, and 22). Regarding claims 7, 15, and 23, Funk et al. teaches a data cache management mechanism that is created by an optimizing compiler. The compiler places non-blocking preload instructions into the instruction stream of the computer system so as to minimize both the frequency and detrimental effect of cache misses (column 3, lines 17-22). Thus, the compiler hopes to minimize cache misses by loading data from the main memory into the cache. This directly relates to the cache loading and replacement scheme of Csoppenszky. The creation of the data cache

management mechanism relates to the claimed material of claims 6,14, and 22, in that a kernel is a core processing mechanism used within a computer system. The optimization compiler of Csoppenszky sends commands for optimizing the caching system as well as controlling the data cache management mechanism, such that parts of the mechanism are present in all mechanism that were compiled by the optimization compiler (column 6, line 66 – column 7, line 11). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Genduso et al. , Csoppenszky and Funk et al. before him at the time the invention was made to modify the caching system of Genduso et al. and Csoppenszky to include the optimization compiler/data cache management mechanism of Funk et al., because then instructions could be pre-loaded into the instruction stream in order to curb the frequency of cache misses, as taught by Funk et al.

Claims 8, 16, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Genduso et al. (US# 5,778,422), Csoppenszky (US# 5,802,568) and Worley, Jr. et al. (US# 4,713,755).

The difference between the claimed subject matter and that of Genduso et al. and Csoppenszky, disclosed supra, is that the claims recite that an instruction for designating replacement is an extension of a memory access instruction. Worley, Jr. et al. teaches a caching system with a corresponding flush data cache instruction. In order to flush, the item must first be selected for removal, hence the extension. The cache line is written back to main memory if the cache line's dirty bit is set (column 4,

lines 36-40). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Genduso et al., Csoppenszky and Worley, Jr. et al. before him at the time the invention was made to modify the caching and clearing scheme of Genduso et al. and Csoppenszky to include the flush data cache instruction of Worley, Jr. et al., because then a system for writing back altered data to the main memory would be in place that would negate the loss of potentially important information, as taught by Worley, Jr. et al.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art corresponds to related cache-based replacement schemes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Brian R. Peugh
Patent Examiner
May 29, 2003